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INTEL/BSTZ
BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KOICHI YAMADA

Appeal 2008-005668
Application 10/607,158
Technology Center 2100

Decided: September 11, 2009

Before JEAN R. HOMERE, ST. JOHN COURTENAY, III, and JAMES R. HUGHES, *Administrative Patent Judges*.

HUGHES, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

This is an appeal under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 1-26. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

Appellant's Invention

Appellant invented a processing method for identifying and terminating error-affected application program threads. (Spec. ¶¶ [0010], [0011.)[1]

Claim

Independent claim 1 further illustrates the invention. It reads as follows:

> 1. A method of terminating an affected application program thread, comprising:
>
> receiving an indication of a hardware error associated with an application program thread;
>
> determining the application program thread to be in a user operation mode; and terminating the application program.

References

The Examiner relies on the following references as evidence of anticipation:

Gilbertson	US 6,594,785 B1	Jul. 15, 2003

[1] We refer to Appellant's Specification ("Spec.") and Appeal Brief ("App. Br.") filed January 25, 2007. We also refer to the Examiner's Answer ("Ans.") mailed July 23, 2007.

(Filed Apr. 28, 2000)

Mathur	US 6,938,254 B1	Aug. 30, 2005 (Filed May 6, 1997)

Rejections

The Examiner rejects claims 1-5, 7-17, 19-24, and 26 under 35 U.S.C. § 102(a) as anticipated by Mathur.

The Examiner rejects claims 6, 18, and 25 under 35 U.S.C. § 103(a) as unpatentable over by Mathur and Gilbertson.

Appellant's Contentions

Appellant contends that the Examiner improperly rejected the claims. Specifically, Appellant contends that the Mathur reference does not disclose any indication of a hardware error, or a hardware error associated with an application program thread (App. Br. 7, 8) – i.e., "receiving an indication of a hardware error associated with an application program thread" (App. Br. 7) as recited in claim 1. Appellant also contends that the combination of the Marthur and Gilbertson references "does not teach or suggest each of the elements of claim 1 and its dependent claim 6" because "Gilbertson does not cure the deficiency of Mathur, which fails to disclose 'receiving an indication of a hardware error associated with an application program thread' recited in base claim 1." (App. Br. 10.) Appellant further contends that "there is no motivation to combine Mathur with Gilbertson." (App. Br. 10.)

Examiner's Findings and Conclusions

The Examiner finds Mathur anticipates Appellant's claims 1-5, 7-17, 19-24, and 26. (Ans. 3-6.) The Examiner finds that Mathur discloses each feature of Appellant's claimed invention, in particular, "receiving an indication of a hardware error associated with an application program thread" as recited in Appellant's claim 1. (Ans. 3, 7-8.) The Examiner also finds that the Marthur and Gilbertson references teach each feature of Appellant's claims 6, 18, and 25. (Ans. 6-7, 8-9.) The Examiner provides a rationale for the reference combination as required by 35 U.S.C. § 103(a), and determined that it would have been obvious for one of skill in the art to combine the references. (Ans. 7, 8-9.)

ISSUES

Based on Appellant's contentions, as well as the findings and conclusions of the Examiner, the issues before us are as follows.

1. Did Appellant establish that the Examiner erred in determining the Mathur reference discloses each feature of Appellant's claimed invention, in particular, receiving an indication of a hardware error associated with an application program thread?

2. Did Appellant establish that the Examiner failed to provide any rationale to combine the Mathur and Gilbertson references?

FINDINGS OF FACT (FF)

We find that the following enumerated findings are relevant to the rejections under review and are supported by at least a preponderance of the

evidence. *Ethicon, Inc. v. Quigg*, 849 F.2d 1422, 1427 (Fed. Cir. 1988) (explaining the general evidentiary standard for proceedings before the Office).

Appellant's Specification

1. Appellant does not explicitly define a "hardware error" in the Specification. Appellant does, however, describe receiving a "machine check abort ('MCA' or hardware error signal)." (Spec. ¶ [0011].) An MCA signal may occur when an error occurs in reading and loading memory data, i.e., from corrupted memory. (Spec. ¶¶ [0021]-[0024].)

Mathur Reference

2. Mathur describes a memory usage control method. The method terminates an application program and its threads when memory usage exceeds a memory utilization threshold (third critical memory usage threshold). (Col. 2, ll. 17-22, 36-42; col. 4, ll. 36-40, 51-66.)

3. Mathur describes the third critical memory usage threshold as the minimum amount of free memory that allows stable computer system operation. When the threshold is met (or exceeded), Mathur prompts a user to terminate an active (executing) application program and freezes all other program activity. (Col. 4, ll. 36-40, 51-66.)

4. Mathur describes notifying (prompting) a user (the user receiving an indication) of an error associated with system memory; i.e., a system hardware error. (Col. 4, ll. 36-40, 51-66.)

5. Mathur also describes freezing the system and notifying a user of the cause of the freeze (exceeding system memory usage limits); i.e., a system hardware error. (Col. 4, ll. 36-40, 51-66.)

PRINCIPLES OF LAW

Burden on Appeal

Appellant has the burden on appeal to the Board to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) ("On appeal to the Board, an applicant can overcome a rejection by showing insufficient evidence of *prima facie* obviousness or by rebutting the *prima facie* case with evidence of secondary indicia of nonobviousness.") (quoting *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998)).

Anticipation

Anticipation is a question of fact. *In re Schreiber*, 128 F.3d 1473, 1477 (Fed. Cir. 1997). Under 35 U.S.C. § 102, "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros., Inc. v. Union Oil Co. of Cal.*, 814 F.2d 628, 631 (Fed. Cir. 1987) (citations omitted); *see also Perricone v. Medicis Pharm. Corp.*, 432 F.3d 1368, 1375 (Fed. Cir. 2005) (citation omitted).

Obviousness

A claimed invention is not patentable if the subject matter of the claimed invention would have been obvious to a person having ordinary skill

in the art. 35 U.S.C. § 103(a); *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007); *Graham v. John Deere Co.*, 383 U.S. 1, 13 (1966).

In *KSR*, the Supreme Court emphasized "the need for caution in granting a patent based on the combination of elements found in the prior art," and stated that "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *KSR*, 550 U.S. at 415-16. The Court explained:

> When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, §103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

Id. at 417. The operative question is thus "whether the improvement is more than the predictable use of prior art elements according to their established functions." *Id.*

Consistent with *KSR*, the Federal Circuit recently recognized that "[a]n obviousness determination is not the result of a rigid formula disassociated from the consideration of the facts of a case. Indeed, the common sense of those skilled in the art demonstrates why some combinations would have been obvious where others would not." *Leapfrog Enters., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1161 (Fed. Cir. 2007) (citing *KSR,* 550 at 416). The Federal Circuit relied in part on the fact that *Leapfrog* had presented no evidence that the inclusion of a reader in the combined device was "uniquely challenging or difficult for one of ordinary

skill in the art" or "represented an unobvious step over the prior art." *Id.* at 1162.

ANALYSIS

Initially, we note the following claim groupings and waiver issues. Appellant does not separately argue claims 2-5, 7-17, 19-24, and 26. (App. Br. 9.) Appellant also does not separately argue claims 18 and 25. (App. Br. 10.) Accordingly, we accept Appellant's grouping of the claims, and we pick claims 1 and 6 as representative claims. *See* 37 C.F.R. § 41.37(c)(1)(vii) ("Notwithstanding any other provision of this paragraph, the failure of appellant to separately argue claims which appellant has grouped together shall constitute a waiver of any argument that the Board must consider the patentability of any grouped claim separately."). We address only those arguments that Appellant presents in the Brief. Arguments that Appellant could have made but chose not to make in the Brief are waived.

Rejection of the Claims under 35 U.S.C. § 102(a)

We decide the question of whether Appellant established that the Examiner erred in determining the Mathur reference discloses each feature of Appellant's claimed invention, in particular, receiving an indication of a hardware error associated with an application program thread. We will affirm the Examiner's rejection of claims 1-5, 7-17, 19-24, and 26 for the reasons that follow.

We find unpersuasive Appellant's contention that Mathur does not provide an indication of a hardware error. We determine the scope of the

claims in patent applications not solely based on the claim language, but upon giving claims "their broadest reasonable interpretation consistent with the specification" and "in light of the specification as it would be interpreted by one of ordinary skill in the art." *In re Am. Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004) (citations omitted). Appellant does not provide any definition for a "hardware error" in the Specification. Appellant, however, does explain that an error may occur from reading data from corrupted memory. In the case of such an error, Appellant describes sending an MCA signal indicating the error. (FF 1.)

We give the term "hardware error" its broadest reasonable interpretation. Accordingly, we find that a hardware error would be commonly understood to mean an error related to computer system hardware, e.g., system memory. Thus, the limitation – an indication of a hardware error – would be commonly understood to be an indication of an error related to system hardware, e.g., system memory. This interpretation is consistent with Appellant's Specification.

Mathur describes terminating an application program and its threads when memory usage meets or exceeds a critical memory usage threshold. When the threshold is met, Mathur prompts a user to terminate an executing application program and freezes all other program activity. (FF 2, 3.) Thus, Mathur describes prompting a user (providing an indication to a user) of an error associated with system memory, and freezing the computer system. (FF 4, 5.) Exceeding a memory usage threshold (causing unstable system performance (FF 3)) and a system "freeze" are system errors related to system hardware (memory), i.e., system hardware error. Appellant's claimed limitation – receiving an indication of a hardware error – is

structurally and functionally equivalent to the method described by Mathur. Appellant's argument that a hardware error is an "error caused by malfunction of a physical component of the computer" is not within the scope of the recited claim limitations, and is therefore irrelevant. (App. Br. 8.)

The Examiner properly explains where each feature of Appellant's claims is shown in the Mathur reference. We agree with the Examiner that Mathur discloses receiving an indication of a hardware error – in particular, a memory error – associated with an application program thread. (Ans. 3, 7-8.) Accordingly, we find that Mathur discloses each feature of Appellant's claims 1-5, 7-17, 19-24, and 26, thus anticipating the claims. Appellant did not file a Reply Brief, nor did Appellant provide any persuasive evidence supporting the assertions of alleged error in the Examiner's position. Accordingly, Appellant has not met the burden to show reversible error in the Examiner's findings. For all the reasons noted above, we will sustain the Examiner's rejection of claims 1-5, 7-17, 19-24, and 26.

Rejection of the Claims under 35 U.S.C. § 103(a)

Appellant does not address the merits of the Examiner's rejection. Thus, we decide the question of whether Appellant establishes the Examiner failed to provide any rationale to combine the Mathur and Gilbertson references. We will affirm the Examiner's rejection of claims 6, 18, and 25 for the reasons that follow.

Appellant briefly contends that the cited Mathur and Gilbertson references do not teach the features of claim 6, restating the arguments made with respect to claim 1, as well as the Mathur reference – that "Gilbertson

does not cure the deficiency of Mathur, which fails to disclose 'receiving an indication of a hardware error associated with an application program thread' recited in base claim 1." (App. Br. 10.) However, this statement is insufficient to rise to the level of a separate argument requiring our consideration. *See Hyatt v. Dudas*, 551 F.3d 1307, 1314 (Fed. Cir 2008) ("When the appellant fails to contest a ground of rejection to the Board, section 1.192(c)(7) [(now section 41.37(c)(1)(vii))] imposes no burden on the Board to consider the merits of that ground of rejection. . . . [T]he Board may treat any argument with respect to that ground of rejection as waived."). *See also In re Guess*, 2009 WL 1598475 at *1 (Fed. Cir. June 9, 2009) ("Appellants failed to argue that any limitations unique to [the claims] survive [the rejection]. Appellants have therefore waived any such arguments on appeal.") (citing *In re Watts*, 354 F.3d 1362, 1367 (Fed. Cir. 2004)).

Appellant merely contends that "there is no motivation to combine Mathur with Gilbertson." (App. Br. 10.) In response, the Examiner explains that it would have been obvious for one of skill in the art to modify the Mathur reference as taught by Gilbertson such that the system receives information of a poisoned memory location (address) in order to isolate and handle memory faults (errors). (Ans. 7, 8-9.)

We agree with the Examiner's rationale for combining Mathur and Gilbertson. The Examiner provides ample evidence of reasons to combine the references. Accordingly, we find the Examiner has "articulated reasoning with some rational underpinning" for the combination of the references. *KSR,* 550 U.S. at 418. Thus, in light of *KSR* and *Leapfrog*, the evidence provided by the Examiner supports a finding that combining

familiar elements according to known methods is obvious when it does no more than yield predictable results.

For all the reasons noted above, Appellant fails to demonstrate error in the Examiner's rejection of claims 6, 18, and 25. Accordingly, we will sustain the Examiner's rejection of these claims.

CONCLUSION OF LAW

On the record before us, we find Appellant has not established the Examiner erred in finding the Mathur reference discloses each feature of Appellant's claimed invention, in particular, receiving an indication of a hardware error associated with an application program thread. We also find Appellant has not established the Examiner failed to provide any rationale to combine the Mathur and Gilbertson references.

DECISION

We affirm the Examiner's rejection of claims 1-5, 7-17, 19-24, and 26 under 35 U.S.C. § 102(a).

We affirm the Examiner's rejection of claims 6, 18, and 25 under 35 U.S.C. § 103(a).

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED

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Intel/BSTZ
Blakely Sokoloff Taylor & Zafman LLP
1279 Oakmead Parkway
Sunnyvale, CA 94085-4040